

**PRE-APPEAL BRIEF REQUEST FOR REVIEW**

Docket Number:

10559-612001

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Application Number

10/039,289

Filed

January 4, 2002

First Named Inventor

Gilbert Wolrich et al.

Art Unit

2177

Examiner

Srirama Channavajjala

Applicant requests review of the rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a Notice of Appeal.

The review is requested for the reason(s) stated on the attached sheet(s).

Note: No more than five (5) pages may be provided.

I am the

☐ applicant/inventor.

☐ assignee of record of the entire interest.
 See 37 CFR 3.71. Statement under 37 CFR 3.73(b)
 is enclosed. (Form PTO/SB/96)

☐ attorney or agent of record 56,569
 (Reg. No.)

☒ attorney or agent acting under 37 CFR 1.34.
 Registration number if acting under 37 CFR 1.34
56,569

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February 14, 2006
 Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below.

☒ Total of 1 forms are submitted.



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Gilbert Wolrich et al. Art Unit : 2166
Serial No. : 10/039,289 Examiner : Srirama Channavajjala
Filed : January 4, 2002
Title : QUEUE ARRAYS IN NETWORK DEVICES

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Commissioner for Patents
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Alexandria, VA 22313-1450

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Pursuant to United States Patent and Trademark Office OG Notices: 12 July 2005 - New Pre-Appeal Brief Conference Pilot Program (extended January 10, 2006), a request for a review of identified matters on appeal is hereby submitted with the Notice of Appeal. Review of these identified matters by a panel of examiners is requested because the rejections of record are clearly not proper and are without basis, in view of a clear legal or factual deficiency in the rejections. All rights to address additional matters on appeal in any subsequent appeal brief are hereby reserved.

Claims 1-37 are pending, with claims 1, 7, 14, 26, 31, 33, 34, and 36 being independent. Claims 1-37 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Regache, Pascal (EP 0760501) in view of Slane (U.S. Patent No. 6,438,651). Applicants respectfully traverse this rejection.

Applicants specifically request the panel to review the following issues:

1. The Examiner has made a clear error in a factual basis to support a *prima facie* case of obviousness for claims 1-30.

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2. The Examiner has omitted at least one essential element needed to support a *prima facie* case of obviousness for claims 31-37.

Each of these issues is discussed in greater detail below. Applicants reserve the right to expand these issues and/or present new issues when filing their appeal brief, including issues raised in previous replies filed on August 9, 2004, January 18, 2005, April 15, 2005, and July 29, 2005, each of which is incorporated herein by reference.

Discussion of Issues:

1. The Examiner has made a clear error in a factual basis to support a *prima facie* case of obviousness for claims 1-30.

The Examiner has made a clear error in factual basis for at least one essential element needed for a *prima facie* rejection of claims 1-30. In view of this error, no proper combination of Pascal and Slane teaches or suggests all limitations of independent claim 1, 7, 14, or 26. Thus, the combination of these references fails to support a *prima facie* case of obviousness with respect to these claims or claims dependent on these claims. In order to establish a *prima facie* case of obviousness, the MPEP § 2141 states:

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations.

Claims 1 recites “storing in memory a plurality of queue descriptors each including a head pointer pointing to a first element in a corresponding queue and a tail pointer pointing to a last element in the corresponding queue” and “fetching from the memory to a cache one of either the head pointer or tail pointer ...”

Claims 7 recites “storing in memory a plurality of queue descriptors each including a head pointer pointing to a first element in a corresponding queue and a tail pointer pointing to a last element in the corresponding queue” and “determining whether a head pointer or a tail

pointer of a queue descriptor that was fetches from the memory to a cache ... had been modified ...”

Claim 14 recites “memory for storing a plurality of queue descriptors, each of which includes a head pointer pointing to a first element in a corresponding queue and a tail pointer pointing to a last element in the corresponding queue” and “a processor configured to: fetch from the memory to the cache one of either the head pointer or the tail pointer ...”

Claims 26 recites “[storing] in memory a plurality of queue descriptors each including a head pointer pointing to a first element in a corresponding queue and a tail pointer pointing to a last element in the corresponding queue” and “[fetching] from memory to a cache one of either a head pointer ... or a tail pointer ...”

With respect to each of these claims 1, 7, 14, and 26, the Office Action cites col. 7, line 14-20 of Pascal to support the Examiner's assertion that Pascal teaches the corresponding limitation requiring that each of a plurality of queue descriptors includes a head pointer and a tail pointer. However, this portion of Pascal reproduced in context below clearly does not support such an assertion.

Figure 3 shows a circular queue 10 formed in paged memory and used to buffer the transfer of data items between a producer entity 12 and a consumer entity 13. The overall arrangement shown in Figure 3 is similar to that of Figure 2 as regards the circular queue itself and the maintenance of head and tail pointers.

Thus, in the Figure 3 arrangement, the producer entity 12 maintains a tail pointer in register 30, this pointer corresponding to the address in memory of the next storage location to be written to. This pointer is maintained within a queue segment (that is, for storage locations within the same memory page) by updating it each time a data item is written by the number of memory addresses occupied by each data item. (col. 7, lines 11-24)

As is evident from the passage above and Figures 2 and 3, Pascal does not describe or even suggest that there is more than one “queue descriptor” (under any consistent interpretation of the claims or prior art teachings) that includes both a head pointer and a tail pointer. Instead, Pascal is concerned with maintaining a single set of head and tail pointers for a single circular queue.

With respect to claims 1, 14, and 26, the Office Action cites col. 9, line 1-15 of Pascal to support the Examiner's assertion that Pascal teaches the corresponding limitation requiring that a head or tail pointer is fetched from the memory to a cache. With respect to claim 7, the Office Action cites fig. 3, col. 7, line 14-16 to support the assertion that Pascal teaches the limitation

reciting that a head pointer or tail pointer was fetched from the memory to a cache. However, neither of these passages even discloses that a cache is used, much less, that a head or tail pointer is fetched from a memory to a cache.

Applicants submit that the Examiner has not properly established a *prima facie* case of obviousness with respect to claims 1-30. For at least these reasons, Applicants respectfully requests withdrawal of the §103(a) rejection of claims 1-30.

2. The Examiner has omitted at least one essential element needed to support a *prima facie* case of obviousness for claims 31-37.

The Examiner has omitted at least one essential element needed for a *prima facie* rejection of claims 31-37. In particular, no proper combination of Pascal and Slane teaches or suggests all limitations of independent claim 31, 33, 34, or 36. Thus, the combination of these references fails to support a *prima facie* case of obviousness with respect to these claims or claims dependent on these claims.

Claim 31 recites “in response to a command to perform an enqueue or dequeue operation with respect to the queue, fetching from the memory to a cache the count and one of either the head pointer or tail pointer.”

Claim 33 recites “returning a count identifying a number of elements in the queue and one of either the head pointer or tail pointer to the memory from the cache only if that pointer had been modified.”

Claim 34 recites “fetch from the memory to the cache the count and one of either the head pointer or the tail pointer of a particular queue descriptor in response to a command to perform an enqueue or a dequeue operation with respect to the particular queue descriptor.”

Claim 36 recites “in response to a command to perform an enqueue or dequeue operation with respect to a queue, fetch from memory to a cache the count and one of either a head pointer pointing to a first element in the queue or a tail pointer pointing to a last element in the queue.”

Nowhere in the Office Action does the Examiner even attempt to point out how the prior art references, alone or combined, teach or suggest any of the limitations recited above. Thus, the Examiner has omitted at least one essential element needed for a *prima facie* §103(a)

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rejection of claims 31-37, namely "the prior art reference (or references when combined) must teach or suggest all the claim limitations."

Applicants submit that the Examiner has not properly established a *prima facie* case of obviousness with respect to claims 31-37. For at least these reasons, Applicants respectfully requests withdrawal of the §103(a) rejection of claims 31-37.

Please apply any charges or credits to deposit account 06-1050.

Respectfully submitted,

Date: 2-14-06



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